



<b>INFORMATION DISCLOSURE CITATION PTO-1449</b>	Atty. Docket No. 050637	Serial No. 10/551,391
	Applicant(s): SASAO, Tsutomu, et al.	
	Filing Date: September 29, 2005	Group Art Unit: Not yet assigned

### U.S. PATENT DOCUMENTS

Examiner Initial		Document No.	Name	Date	Class	Subclass	Filing Date (If appropriate)
_____	AA	Re. 34,363	R. H. Freeman	08/31/1993			
_____	AB						

### FOREIGN PATENT DOCUMENTS

		Document No.	Date	Country	Translation (Yes or No)
_____	AC				
_____	AD				

### OTHER DOCUMENTS

_____	AE	T. Sasao et al., "A Cascade Realization of Multiple-Output Function and Its Application to Reconfigurable Hardware," The Institute of Electronics, Information and Communication Engineers, Vol. 101, No. 3, Mie University, FTS2001-8, April 2001, pp. 57-64. English abstract is included. Discussed in the specification.
_____	AF	T. Sasao et al. "A Cascade Realization of Multiple-Output Function for Reconfigurable Hardware" International Workshop on Logic and Synthesis (IWLS01), Lake Tahoe, CA, June 12-15, 2001, pp. 225-230 w/cover page and the TOC, Discussed in the specification.
_____	AG	A. Tomita et al., "A Design of LUT-Array-Based PLD," The Institute of Electronics, Information and Communication Engineers, Vol. 100, No. 475, November 2000, pp. 173-178. English abstract is included.

Examiner	Date Considered
----------	-----------------



INFORMATION DISCLOSURE CITATION PTO-1449	Atty. Docket No. 050637	Serial No. 10/551,391
	Applicant(s): SASAO, Tsutomu, et al.	
	Filing Date: September 29, 2005	Group Art Unit: Not yet assigned

#### OTHER DOCUMENTS

_____	BA	Y. Iguchi et al., "Realization of Multiple-Output Functions by Reconfigurable Cascades, " International Conference on Computer Design :VLSI in Computers & Processors (ICCD-2001), Austin, TX, Sept. 23-26, 2001. pp. 388-393 (published page number).
_____	BB	A. Mishchenko et al., "Encoding of Boolean Functions and Its Application to LUT Cascade Synthesis, " International Workshop on Logic and Synthesis (IWLS2002), New Orleans, Louisiana, June 4-7, 2002, pp.115-120.
_____	BC	T. Sasao, "Design Methods for Multi-Rail Cascades," International Workshop on Boolean Problems (IWBP2002), Freiberg, Germany, Sept. 19-20, 2002, pp. 123-132.
_____	BD	T. Sasao et al., "A Design Method for Irredundant Cascades," International Symposium on New Paradigm VLSI Computing, Sendai, Japan, Dec. 12-14, 2002, pp.37-40.
_____	BE	A. Mishchenko et al., "Logic Synthesis of LUT Cascades with Limited Rails," The Institute of Electronics, Information and Communication Engineers, Lake Biwa, VLD2002-99, November 2002, pp. 1-6.
_____	BF	H. Gouji et al., "On a Method to Reduce the Number of LUTs in LUT cascades," The Institute of Electronics, Information and Communication Engineers, Kitakyushu, VLD2001-99, November 2001, 6 sheets, English abstract is included.
_____	BG	M. Matsuura et al., "Compact Representaions of BDDs for Multiple-Output Functions and Their Optimization," The Institute of Electronics, Information and Communication Engineers, Kitakyushu, VLS2001-100, November 2001, 6 sheets, English abstract is included.
Examiner _____ Date Considered _____		